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Estimating Power for ADSP-BF533 Blackfin® Processors

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Rev 1 – February 20, 2004

Introduction

This EE-Note discusses the methodology for estimating total average power consumption on the ADSP-BF533 Blackfin® family of processors (including the ADSP-BF531 and ADSP-BF532 derivatives). The following documentation will detail how to interpret power measurements published in the processor data sheet and how to extrapolate data for individual sets of operating conditions based on measured data at specific operating conditions. A "worst-case" scenario is also made available as an example for board designers to consider when designing their power supplies.

Average Power Consumption

Total average power consumption (P_{DDTOT}) is the sum of the average power dissipated in each of the three power domains in a Blackfin application: internal supply (V_{DDINT}), external supply (V_{DDEXT}), and, optionally, Real-Time Clock supply (V_{DDRTC}). There are different supply voltages because the core does not operate at the same voltage as the I/O. The core operates within the range of 0.8-1.32V with a nominal rating of 1.2V (V_{DDINT}). The I/O circuitry supports a range of 2.25-3.6V with a nominal rating of 2.5V or 3.3V (V_{DDEXT}), depending on the system. The Real-Time Clock can be powered by the I/O supply but, if the user wanted to absolutely maximize power savings, it could be the case that both V_{DDINT} and V_{DDEXT} are powered off. The Hibernate power mode on the ADSP-BF533 processor allows power to be removed from the core and, optionally, removed from the I/O. To allow a Real-Time Clock event to restore power to the core after exiting Hibernate mode, the Real-Time Clock must remain powered by a separate supply, such as a battery. A third power domain (V_{DDRTC}) satisfies this need.

Since power is defined as the product of the supply voltage and the current drawn, the power domains are described by the equations:

$$P_{DDINT} = V_{DDINT} * I_{DDINT}$$
$$P_{DDEXT} = V_{DDEXT} * I_{DDEXT}$$
$$P_{DDRTC} = V_{DDRTC} * I_{DDRTC}$$

For the purposes of this document, current and power values are treated as average values and voltages are assumed to be constant. The total average power dissipated by the processor is the sum of three components:

$$P_{DDTOT} = P_{DDINT} + P_{DDEXT} + P_{DDRTC}$$

The following sections describe how to estimate each of the three components.

Average Internal Power Consumption

There are a few things to consider when estimating the average internal power dissipation of a processor. The first consideration is the fact that internal power is composed of two components, one static and one dynamic.

The static component, as the name implies, is independent of transistor switching frequency. It

is a reflection of "leakage" current, which is a phenomenon that causes transistors to dissipate power even when they are not switching. Leakage is a factor in high-performance CMOS circuit design and is a function of both the supply voltage and the ambient operating temperature at which the part is expected to run. Leakage current increases as temperature and/or voltage increases.

The dynamic power component is largely independent of temperature and is a function of supply voltage and switching frequency. The faster the transistors can switch, the more voltage swings occur. The higher the supply voltage, the larger the voltage swing between the on and off transistor states. Thus, the dynamic component will increase with voltage and/or frequency.

The second major consideration in estimating average internal power is the type of application code expected to run on the processor. Specifications in the data sheet were obtained while the processor ran a 75% Dual-MAC and 25% Dual-ALU algorithm, which was fetching slowly changing data from L1 data memory. All peripherals were disabled, but the core and L1 memory were running. To help the board designer "size" the voltage regulators, power numbers under full stress conditions are provided in this document. These conditions include the core running an algorithm consisting of 100% Dual-MACs and more strenuous data-switching characteristics. This is discussed in more detail in the "Estimating Average Static Power" section of this document.

Finally, the actual power numbers can fluctuate within a defined range based on the processor fabrication process at the transistor geometries required for such high speeds. This is largely due to the semiconductor doping process (i.e., ion implantation), which does not result in uniform connectivity among the transistors, yielding slight variations of the die in any given wafer of silicon. Other physical phenomena related to the fabrication process also contribute to this non-uniformity. These physical differences cause some die to conduct faster than others, which results in three process-related groupings. Figure 1 shows a process curve, which is a graphical representation of this categorization based upon transistor threshold voltage (V_T) and saturation current (I_{DDSAT}).

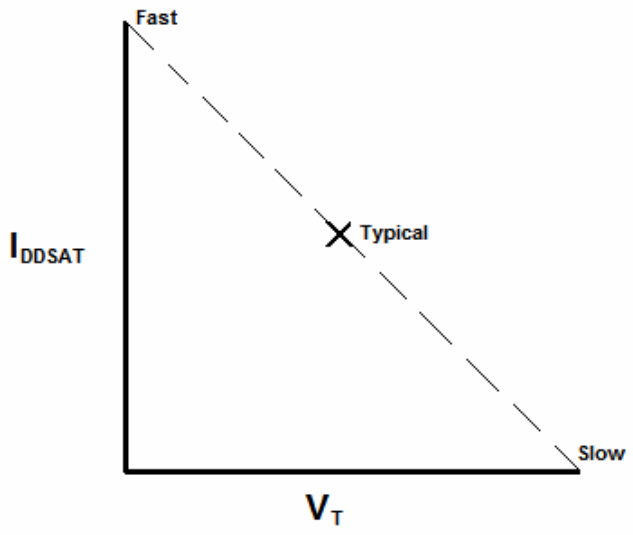

Figure 1. Process Curve (I_{DDSAT} vs V_T)

The process contains three "corners": fast, typical, and slow. A "fast corner" part results when the threshold voltage is minimized and the saturation current is highest. Conversely, a "slow corner" part has high threshold voltage and low saturation current. Although "fast corner" parts allow for higher operating frequencies, the trade-off is higher leakage current and higher dissipated power in general.

Estimating Average Static Power

The static component for average internal power is a result of the leakage current that occurs even when the transistors are not changing state. When the clocks (core and system) are off and voltage is applied to the core and L1 memory, Blackfin processors are in "Deep Sleep" mode. The data sheet shows the $I_{DDDEEPSLEEP}$ measurement to indicate the static current component that contributes to the internal static power consumption (P_{DDINT_ST}):

$$P_{DDINT\_ST} = V_{DDINT} * I_{DDDEEPSLEEP}$$

Table 1 shows the "Internal Power Dissipation" table from the *ADSP-BF531/BF532/BF533 Blackfin Embedded Processor Data Sheet* [1]. This table contains average internal current draw measurements, which were taken from a representative sample of typical parts. In terms of the static current component, $I_{DDDEEPSLEEP}$, the ambient temperature that yielded these numbers was 25°C, denoted by footnote 2. The table shows that the drawn current increases when the voltage rises from 0.8V to 1.2V. Although no direct correlation between voltage increases and leakage can be made, the table sufficiently details the leakage that can be expected within the acceptable voltage range at 25°C for "typical corner" parts.

Parameter	Test Conditions[2]				Unit
	f_{CCLK} = 50 MHz, V_{DDINT} = 0.8 V	f_{CCLK} = 400 MHz, V_{DDINT} = 1.2 V	f_{CCLK} = 500 MHz, V_{DDINT} = 1.2 V	f_{CCLK} = 600 MHz, V_{DDINT} = 1.2 V	
I_{DDTYP}[3]	26	160	190	220	mA
$I_{DDSLEEP}$[4]	16	37	37	37	mA
$I_{DDDEEPSLEEP}$[4]	14	31	31	31	mA
$I_{DDHIBERNATE}$[5]	50				µA
I_{DDRTC}[6]	30				µA

[1] See EE-229: Estimating Power On The BF533/2/1 Blackfin Processors.
[2] I_{DD} data is specified for typical process parameters. All data at 25°C.
[3] Processor executing 75% dual Mac, 25% ADD with moderate data bus activity.
[4] See the *ADSP-BF53x Blackfin Processor Hardware Reference Manual* for definitions of Sleep and Deep Sleep operating modes.
[5] Measured at V_{DDEXT} = 3.65V with voltage regulator off (V_{DDINT} = 0V).
[6] Measured at V_{DDRTC} = 3.3V at 25 25°C.

Table 1. Internal Power Dissipation (Typical)

To help size the power supply, a set of faster, higher leakage parts were measured. Table 2 is similar to Table 1, except that it focuses on parts that have higher leakage current, which are very close to a worst-case average internal power dissipation scenario in terms of silicon type with no DMA and no peripherals enabled.

The ambient temperature is still 25°C, as the maximum 85°C example is addressed in the "Worst-Case Model" section of this note. Additionally, these numbers reflect average internal power dissipated when the core is running a 100% Dual-MAC algorithm, which maximizes the workload on the core but is not typical application code.

Parameter	Test Conditions			Unit
	f_{CCLK} = 400 MHz, V_{DDINT} = 1.2 V	f_{CCLK} = 500 MHz, V_{DDINT} = 1.2 V	f_{CCLK} = 600 MHz, V_{DDINT} = 1.2 V	
I_{DDFAST}	278	312	347	mA
$I_{DDDEEPSLEEP}$	120	120	120	mA

Table 2. Average I_{DDINT} on Faster Part (1.2V)

The average internal power consumption data is an *average* measurement of the representative sample of faster, higher leakage parts. Therefore, some parts from within this sample yielded power measurements that slightly exceed the estimations presented in this document as "worst-case".

As can be extrapolated in the comparison between Table 1 and Table 2, leakage current can increase in magnitude by a factor of four due to normal semiconductor processing variations. Note that the current draw in Table 2 is labeled I_{DDFAST} to differentiate between the current draw from typical parts (I_{DDTYP}) and the current draw obtained on faster, higher leakage parts.

Another important factor relative to leakage current is ambient temperature. Static power consumption increases exponentially with ambient temperature, as detailed by the equation:

$$P_{DDINT\_ST@T} = P_{DDINT\_ST@T0} * e^{(0.015 * (T - T0))}$$

where $P_{DDINT\_ST@T0}$ is the power dissipated due to leakage current at the known temperature ($T0$) and $P_{DDINT\_ST@T}$ is the unknown number at the target temperature (T). Using Table 2, the static component of 120mA, given at $T0 = 25°C$, can be multiplied by the supply voltage (1.2V) to obtain the $P_{DDINT\_ST@T0}$ value of 144mW. Since the goal is

to estimate the worst-case scenario in terms of temperature, the target temperature T is 85°C. Given these known values, the estimate for $P_{DDINT\_ST@T}$ can now be calculated:

$$P_{DDINT\_ST@85°C} = 144mW * e^{(0.015 * (85 - 25))}$$
$$= 144mW * 2.4596$$
$$= 354.183mW$$

To compare to the values detailed in Table 2, extract the current component:

$$I_{DDDEEPSLEEP@85°C} = P_{DDINT\_ST@85°C} / V_{DDINT}$$
$$= 354.183mW / 1.2V$$
$$= 295mA$$

The actual average measurement on a set of faster parts under these conditions yielded:

$$I_{DDDEEPSLEEP@85°C} = 302mA$$

As shown, the exponential estimate is within 3% of the measured value. For those who do not care for exponents, it is observed that the leakage current roughly doubles for every 50°C increase in ambient temperature. In other words:

$$I_{DDDEEPSLEEP@75°C} = 2 * I_{DDDEEPSLEEP@25°C}$$
$$= 2 * 120mA$$
$$= 240mA$$

Since the temperature increase from 25°C to 85°C is greater than 50°C, the baseline for the doubling leakage current changes from the known value at 25°C to the estimated value at 75°C. The same "doubles over 50°C" theory is applied again, knowing that the increase is now 10°C instead of 50°C, which is 20% of the 50°C used in the doubling estimation. Therefore, the estimated leakage at 85°C is roughly a 20% increase over the estimated leakage at 75°C:

$$I_{DDDEEPSLEEP@85°C} = 1.2 * I_{DDDEEPSLEEP@75°C}$$
$$= 1.2 * 240mA$$
$$= 288mA$$

This method, while not as accurate as the exponential estimate, is still within an error of 5% and is a fairly accurate mathematical model. The "doubling" estimate is not linear, so the error increases once the 20% assumption is made.

In summary, these methods can be applied for the acceptable ambient temperature range once a baseline "Deep Sleep" mode current measurement is obtained from the part in question at the operating voltage of choice. Also, please recall that these measurements and estimations are *averages* across a representative sample of parts.

Estimating Average Dynamic Power

The dynamic component of average internal power is a function of the operating frequency and the supplied voltage. Remember that the values in Table 2 are from a set of faster, higher-leakage parts and represent the maximum current drawn at 1.2V and 25°C on a fully-loaded core. The process of extrapolating measurements by virtue of frequency and voltage scaling will now be discussed.

Table 2 shows the I_{DDFAST} measurements at three frequencies with $V_{DDINT} = 1.2V$. Using two measurements in the table, one can calculate the ratio of current draw increase to frequency increase. For example, the 400MHz measurement for I_{DDFAST} is 278mA and the 500MHz measurement is 312mA. The ratio is 34mA per 100MHz, which can be seen between 500 and 600MHz as well. Once this ratio is known, the expected current draw can be calculated at any frequency:

$$I_{DDINT@F} = I_{DDINT@F0} + [(F - F0) * Ratio]$$

where F is the target frequency, $F0$ is the known frequency, and $Ratio$ is the change in current draw per change in frequency. Given this model, to estimate the total current drawn at 600MHz:

$$I_{DDFAST600} = I_{DDFAST400} + [(600 - 400) * (34/100)]$$
$$= 278 + 68$$
$$= 346mA$$

Comparing this estimated value with the measured value at 600MHz (347mA), the

estimate is within 1% of the actual data. In this model, Ratio is applied only as a dynamic current adjustment to the total measured current draw at a different frequency. Since the static current component is independent of frequency and is already included in the $I_{DDFAST400}$ measurement, it is not impacted by this adjustment.

A second extrapolation from the data in Table 2 is known as "frequency scaling". A common question regarding frequency scaling is "Why is the current draw at 600MHz not equal to 1.5 times the value obtained at 400MHz?". The basis for this question is understandable because the ratio from 400MHz to 600MHz is 1.5. However, the answer is based on the fundamental understanding that the static power component is not affected by a change in frequency. In Table 2, the measured value I_{DDFAST} contains both the static and dynamic components:

$$I_{DDFAST} = I_{DDDEEPSLEEP} + I_{DDFAST\_DYN}$$

where $I_{DDDEEPSLEEP}$ is the leakage, which remains constant across the frequency domain, and I_{DDFAST_DYN} is the dynamic component, which *is* affected by changes in frequency. Since the intent is to apply the dynamic power ratio to the current draw measurement, the static component must be removed prior to performing this operation:

$$\begin{aligned} I_{DDFAST\_DYN400} &= I_{DDFAST400} - I_{DDDEEPSLEEP} \\ &= 278 - 120 \\ &= 158mA \end{aligned}$$

Because the frequency is being increased by a factor of 50%, the dynamic ratio can be applied:

$$\begin{aligned} I_{DD\_DYN600} &= 1.5 * I_{DD\_DYN400} \\ &= 1.5 * 158 \\ &= 237mA \end{aligned}$$

At this point, the static component can be added back in, yielding a total estimated current drawn:

$$\begin{aligned} I_{DDFAST600} &= I_{DDDEEPSLEEP} + I_{DD\_DYN600} \\ &= 120 + 237 \\ &= 357mA \end{aligned}$$

This estimate falls within an error of 3% of the measured data of 347mA.

Aside from the frequency factor, the dynamic component is also affected by changes in supply voltage. Another extrapolation method called "voltage scaling" can be applied to estimate power when V_{DDINT} is changing. Table 3 depicts the same data as Table 2, only now the supply voltage has been increased 10% to the nominal V_{DDINT} of 1.32V. The other parameters are the same (i.e., application is 100% Dual-MACs, and ambient temperature is 25°C):

Parameter	Test Conditions			Unit
	f_{CCLK} = 400 MHz V_{DDINT} = 1.32V	f_{CCLK} = 500 MHz V_{DDINT} = 1.32V	f_{CCLK} = 600 MHz V_{DDINT} = 1.32V	
I_{DDHIGH}	328	368	409	mA
$I_{DDDEEPSLEEP}$	150	150	150	mA

Table 3. Average I_{DDINT} on Faster Part (1.32V)

Note that the nomenclature for the current draw has changed to I_{DDHIGH} to indicate that these numbers were obtained under the same conditions as I_{DDFAST}, except now they are a result of the highest allowed V_{DDINT}. Using Tables 2 and 3, one can obtain the two measurements taken at 400MHz for the typical current draw value:

$$I_{DDFAST400} = 278mA$$
$$I_{DDHIGH400} = 328mA$$

Again, these numbers are a combination of the static and dynamic components, so the static component must be removed first:

$$I_{DDFAST400\_DYN} = 278 - 120 = 158mA$$
$$I_{DDHIGH400\_DYN} = 328 - 150 = 178mA$$

The ratio of dynamic power consumption from one applied voltage to another is directly

proportional to the square of the voltage ratio itself, or:

$$P_{DDHIGH\_DYN} = P_{DDFAST\_DYN} * (1.32V/1.20V)^2$$
$$= (1.2V * 158mA) * (1.21)$$
$$= 229.416mW$$

The current component is easily extracted by dividing this value by the supply voltage:

$$I_{DDHIGH\_DYN} = P_{DDHIGH\_DYN} / 1.32V$$
$$= 229.416mW / 1.32V$$
$$= 173.8mA$$

Now the static component at 1.32V can be added:

$$I_{DDHIGH} = I_{DDHIGH\_DYN} + I_{DDHIGH\_DEEPSLEEP}$$
$$= 173.8 + 150$$
$$= 323.8mA$$

The estimated value is within 2% of the actual value of 328mA. The total current draw can then be used to calculate the average internal power consumption:

$$P_{DDHIGH} = I_{DDHIGH} * V_{DDINT}$$
$$= 323.8mA * 1.32V$$
$$= 427.4mW$$

These extrapolation methods can be taken a step further by applying both the frequency and voltage scales with one equation. Since the frequency ratio is linear, it can be factored into the equation used for voltage scaling:

$$P_{DDDYN@V} = P_{DDDYN@V0} * (V/V0)^2 * (F/F0)$$

where $V0$ is the reference voltage, V is the target voltage, $F0$ is the reference frequency, and F is the target frequency. For example, the current values in Table 2 at $F0=400MHz$ and $V0=1.2V$ are known and the wish is to obtain the estimated measurements at $F=600MHz$ and $V=1.32V$. Again, the first step is to remove the static component:

$$I_{DDFAST400\_DYN} = 278 - 120 = 158mA$$

Second, the known values are substituted into the equation:

$$P_{DDDYN@V} = P_{DDDYN@V0} * (V/V0)^2 * (F/F0)$$
$$P_{DDHIGH\_DYN} = P_{DDFAST\_DYN} * (1.32/1.2)^2 * (600/400)$$
$$= (1.2V * 158mA) * 1.815$$
$$= 344.124mW$$

The current component is easily extracted by dividing this value by the supply voltage:

$$I_{DDHIGH\_DYN} = P_{DDHIGH\_DYN} / 1.32V$$
$$= 344.124mW / 1.32V$$
$$= 260.7mA$$

Now the static component at 1.32V can be added:

$$I_{DDHIGH} = I_{DDHIGH\_DYN} + I_{DDHIGH\_DEEPSLEEP}$$
$$= 260.7 + 150$$
$$= 410.7mA$$

The estimated value is within 0.5% of the actual measured value of 409mA. The value can then be used to calculate the average internal power consumption:

$$P_{DDHIGH} = I_{DDHIGH} * V_{DDINT}$$
$$= 410.7mA * 1.32V$$
$$= 542.1mW$$

In summary, there are many methods available to estimate internal power consumption based on the values presented in the data sheet *or* on values obtained under nominal conditions when considering worst-case operating conditions.

Average External Power Consumption

Average external power dissipation is the average power dissipated in the V_{DDEXT} power domain. The number of components that contribute to the overall external power value is the number of enabled peripherals in a given system. Each unique group of peripheral pins contributes to a piece of the overall external power based upon several parameters:

- Number of output pins (O)
- Number of pins toggling each clock cycle (TR)
- Frequency at which the peripheral runs (f)
- Utilization factor - percentage of time that the peripheral is on (U)
- Load capacitance (C)
- Voltage swing (V_{DDEXT})

The equation used to derive each component's contribution to the total external power is:

$$P_{DDEXT} = (V_{DDEXT})^2 * C * f/2 * (O*TR) * U$$

The worst external pin power scenario is when the load capacitor continuously charges and discharges, requiring the pin to toggle continuously. Since the state of the pin can change only once per cycle, the maximum toggling frequency is f/2. In terms of supply power, the worst-case V_{DDEXT} value is 3.65V. Table 4 contains data for a realistic example of a PPI application, which runs several peripherals simultaneously. Actual results may vary, but again, the intent is to help designers size the power supplies.

Peripheral	Freq (Hz)	# of pins	C/pin (F)	Toggle Ratio	Util	Vddext (V)	Pout @ 3.65V (mW)
PPI	2.70E+07	9	3.00E-11	1	1.00	3.65	48.56
SPORT0	4.00E+06	2	3.00E-11	1	1.00	3.65	1.60
SPORT1	4.00E+06	2	3.00E-11	1	1.00	3.65	1.60
UART	1.15E+05	2	3.00E-11	1	0.25	3.65	0.01
SDRAM	1.33E+08	36	3.00E-11	0.25	0.50	3.65	119.60
Total External Power Dissipation @ 3.65V (est mW)							**171.37**

Table 4. Sample Calculation For Total Average External Power

In the above example, the total average external power consumption is estimated to be ~170mW. This number was obtained with the parameters listed in Table 4 by applying the P_{DDEXT} equation given above. Notice that the recommended load capacitance of 30pF when the V_{DDEXT} is 3.65V was used in this calculation. The chosen operating frequencies are reasonable for each of the peripherals, including the maximum allowed SDRAM frequency of 133MHz. This model assumes that each output pin changes state every clock cycle, which is a worst-case model, except in the case of the SDRAM (because the number of output pins transitioning each clock cycle will be less than the maximum number of output pins). Table 4 was taken from *External Power Spreadsheet* [2], which is associated with this EE-Note. It contains calculations for four sample systems. The reader can tailor this spreadsheet to their application, adding or deleting rows as necessary. Since the equation provides results in Watts (W), an additional scale factor of 1000 in the spreadsheet converts results into mW.

This second equation is a more theoretically accurate version of the one used in the spreadsheet:

$$\overline{P}_{ext} = V_{DDext}{}^2 \cdot \sum_{All-Output-Pins} C_L \cdot \overline{f}$$

Rather than estimating average external power dissipated in each *peripheral*, the estimate applies to each *individual output pin*, based on the pin's load capacitance and average toggling frequency. The voltage swing is uniform across all output pins within the V_{DDEXT} supply domain, so it is multiplied by the summation of the dynamic charge changes on each output.

Using the PPI data in Table 4, nine output pins change every cycle at an average frequency of 27MHz. Since toggling between on-to-off and off-to-on requires two cycles, F_{AVG} is half the PPI clock (13.5MHz). Since each pin changes at the same rate and the pin capacitance is, presumably, the same, the summation is simply nine times the value of any one PPI pin:

$$P_{EXT\_AVG} = V_{DDEXT}^2 * 9 \text{ pins} * (F_{AVG} * C_L)$$
$$= (3.65)^2 * 9 * 13.5e6 * 30e\text{-}12$$
$$= 13.3225 * 0.003645$$
$$= 0.048561W$$
$$= 48.561mW$$

As can be seen, the value derived using this equation is the same as the value estimated in Table 4. This model obtains the same estimate on a per-pin basis rather than a per-peripheral basis.

Finally, a board designer must also be mindful of power supply efficiency when sizing the V_{DDEXT} supply. Refer to *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228)* [3] for more details regarding the Internal Voltage Regulator.

Real-Time Clock (RTC) Power Consumption

The final source of total power consumption comes from the optional third power domain, the Real-Time Clock power domain (V_{DDRTC}), which is a specified value. The RTC can be powered between 2.25V and 3.6V. For a worst-case analysis, a supply voltage of 3.65V yields a current draw of 30-50µA for a range of ambient temperature from 25°C to 85°C. For the sake of including this number in the final "Worst-Case Model", the power consumption is:

$$P_{DDRTCMAX} = V_{DDRTCMAX} * I_{DDRTCMAX}$$
$$= 3.65V * 50\mu A$$
$$= 182.5\mu W$$

Knowing this value also helps in selecting a battery as a potential power source for the RTC. The RTC can be used to take the ADSP-BF533 processor out of any of the low-power operating modes. Having a battery supply the V_{DDRTC} domain allows the removal of the V_{DDINT} and V_{DDEXT} supplies, thus significantly reducing total average power consumption.

Worst-Case Model

To help size voltage regulators, let's consider the worst-case conditions under which an ADSP-BF533 processor might operate (maximum supply voltage, maximum ambient temperature, and maximum operating frequency). To further stress the part, a full load of 100% Dual-MAC operations would be performed by the core and the part under scrutiny would be the faster, higher leakage type. Table 3 shows the current drawn with all of the parameters maximized *except* the ambient temperature. Table 5 contains the same measurements taken at the maximum ambient temperature, 85°C.

Parameter	Test Conditions			Unit
	f_{CCLK}= 400 MHz V_{DDINT}= 1.32V	f_{CCLK}= 500 MHz V_{DDINT}= 1.32V	f_{CCLK}= 600 MHz V_{DDINT}= 1.32V	
I_{DDMAX}	538	579	623	mA
$I_{DDDEEPSLEEP}$	362	362	362	mA

Table 5. Maximum I_{DDINT} (Extreme Conditions)

The current draw is now represented as I_{DDMAX} to differentiate between the current measurements under these extreme conditions versus those obtained in previous data sets. These numbers do not include DMA or peripheral activity, but it is estimated that the internal power dissipation will increase by a maximum of 10% with these additional parameters. Characterization tests are being conducted to identify what sort of power draw increase might be expected in the internal power domain when peripherals are enabled, but two stipulations exist that may deem these increases negligible.

First, the application being run to generate these I_{DDMAX} numbers is not realistic because it keeps a

full load on the core 100% of the time, which is not indicative of a real application.

Second, peripheral hardware activity and DMA will cause stalls in the code being executed by the "fully-loaded" core, which will save power in the core dissipation when small increases in dissipation are being introduced elsewhere on-chip. Given these facts, the measurements in Table 5 should be considered as the worst-case scenario.

From this data, the extreme worst case for total power dissipation can be estimated, assuming all the conditions in Table 5 are met, for the P_{DDMAX} component. The external power component, P_{DDEXT}, is the example used in the "Average External Power Consumption" section of this document and the Real-Time Clock component implies a maximum V_{DDRTC} of 3.65V and ambient temperature of 85°C.

The ADSP-BF533 is available in two speed grades, 500MHz and 600MHz. Although the 500MHz part can be run up to 85°C, the 600MHz part is specified up to 70°C. Therefore, the "worst-case" conditions vary between the two.

Using the data in Table 5 and given all of these assumptions, the total power dissipation, P_{DDTOT}, can be estimated for the 500MHz part:

$$P_{DDTOT500} = P_{DDMAX500} + P_{DDEXT} + P_{DDRTC}$$
$$= (579mA*1.32V) + 171.37mW + 182.5\mu W$$
$$= (764.28 + 171.37 + 0.1825)mW$$
$$= \sim 936mW$$

For the 600MHz part, the measured current drawn at 85°C includes a leakage component of 362mA. Since the dynamic power component remains the same across the temperature domain, it can be separated out:

$$I_{DDMAX\_DYN600} = I_{DDMAX600} - I_{DDDEEPSLEEP}$$
$$= 623 - 362$$
$$= 261mA$$

The static power component can then be used with the exponential temperature model from the "Estimating Average Static Power" section to estimate the leakage at 70°C:

$$P_{DDMAX\_ST@70°C} = P_{DDMAX\_ST@85°C} * e^{(0.015 * (T - T0))}$$
$$= (362mA * 1.32V) * e^{(-0.225)}$$
$$= 477.84mW * 0.7985$$
$$= 381.563mW$$

The current component is easily extracted by dividing this value by the supply voltage:

$$I_{DDDEEPSLEEP@70°C} = P_{DDMAX\_ST@70°C} / V_{DDINT}$$
$$= 381.563mW / 1.32V$$
$$= 289.063mA$$

Now that both the static and dynamic current components are known, a total current draw can be calculated and used to estimate total average power:

$$P_{DDMAX600} = (I_{DDDEEPSLEEP@70°C} + I_{DDMAX\_DYN600}) * V_{DDINT}$$
$$= (289.063 + 261)mA * 1.32V$$
$$= 550.063mA * 1.32V$$
$$= 726.083mW$$

The total power dissipation, P_{DDTOT}, can now be estimated for the 600MHz part:

$$P_{DDTOT600} = P_{DDMAX600} + P_{DDEXT} + P_{DDRTC}$$
$$= 726.1mW + 171.4mW + 182.5\mu W$$
$$= (726.1 + 171.4 + 0.2)mW$$
$$= \sim 898mW$$

These numbers are certainly not typical power consumption numbers. Rather, they may occur if all the critical parameters are maximized, the application code fully stresses the core, and the part is the faster, higher-leakage variety. These numbers are being supplied to aid in specifying the maximum power requirements for a particular system's voltage regulator.

Conclusions

Several variables affect the power requirements of an embedded system. Measurements published in the ADSP-BF533 data sheet are indicative of typical parts running under typical conditions. However, these numbers do not necessarily reflect the actual numbers that may occur for a given processor under non-typical conditions. The fabrication process plays a large role in the total estimated power calculations that are feasible for the ADSP-BF533. In addition to the type of silicon that the customer could have, the ambient temperature, core and system frequencies, supply voltages, pin capacitances, power modes used, application code, and peripheral utilization all contribute to the average total power that may be dissipated.

Even with all the estimates discussed in this document, the result is an estimated average power consumption number at any given time. Assuming that a system can be in several possible states, calculating a true average power dissipation, the user would be required to run a statistical analysis to determine what percentage of the time the processor spends in each of the defined states, apply those percentages to the estimated power consumption calculated for that state, and then add each of the state averages. For example:

```
STATE1 = 20% of application
STATE2 = 10% of application
STATE3 = 70% of application
```

For example, if statistical analysis yields the numbers above for percentage of time spent in a particular system state, the total average power (P_{TOT}) is summarized as follows:

$$P_{TOT} = (0.2*P_{STATE1}) + (0.1*P_{STATE2}) + (0.7*P_{STATE3})$$

The average power number that results from this equation shows how much the Blackfin processor is loading a power source over time. Do not use this calculation to size the power supply! The power supply must support peak requirements.

Average power estimates are useful in terms of expected power dissipation within a system, but designs must support the worst conditions under which the application can be run.

References

[1] *ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Embedded Processor Preliminary Data Sheet.* Rev. PrC, January 2004. Analog Devices, Inc

[2] *External Power Spreadsheet.* Associated file with *Estimating Power for ADSP-BF533 Blackfin Processors (EE-229)* February 2004. Analog Devices, Inc.

[3] *Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors (EE-228).* Rev 1, Available March 2004. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – February 20, 2004 by Joe B.	Initial Release